ASIC Data Acquisition System; Implementation of HINP16C on SAND

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ABSTRACT

Silicon-based particle detectors can be made to be highly segmented with a large surface area, allowing the detector to produce vast amounts of information in the form of energy and timing signals. In order to process so much information, high density signal processing is required. The signals emitted from the particle detector must be amplified and shaped before they can be converted for use by a computer. The traditional readout setup for particle detectors requires separate modules to accomplish the tasks of amplifying, shaping, and converting the signal, and a single channel on a detector requires each of these modules. If highly segmented silicon arrays are being used in an experiment, the traditional setup can be incredibly expensive and impractical. The Application Specific Integrated Circuit (ASIC) system, in comparison to the traditional setup, is far more cost-efficient when used in experiments that require highly segmented silicon arrays. The ASIC system at the University of Notre Dame allows researchers to use up to 512 channels to process the energy and timing signals produced by the detector, all within a box of approximately 40 x 15 x 10 cm in volume. We tested linearity, resolution, and quality of the chips (HINP 16C) used in the ASIC system. This system will be used with a new silicon detector array (SAND), developed at Notre Dame.

1 Background Information

1.1 The Particle Detection System

When a charged particle strikes a semiconductor-based particle detector, electrons in the detector are displaced and the structure of the material is disturbed. This event results in a flow of charge along a narrow strip made up of a conducting

material (aluminum is often used), and the charge is measured by a sensitive electronic readout channel at the end of strip[3]. The signal is amplified, shaped, and converted to a digital format by a series of modules and then interpreted by a computer to determine certain characteristics of the particle. Such characteristics include the kinetic energy, momentum, and velocity of the particle, and the time when the event occurred.

A signal produced by a collision with the detector must be processed by a series of modules before it can be interpreted by a computer. First, the signal is extracted from the detector by the preamplifier. This must be done without significantly degrading the signal-to-noise ratio (SNR), so the preamplifier is located as close as possible to the detector. From the preamplifier, the information is relayed in the form of energy and timing signals. The energy signal feeds the E-train branch for processing, while the timing signal feeds the T-train branch[2].

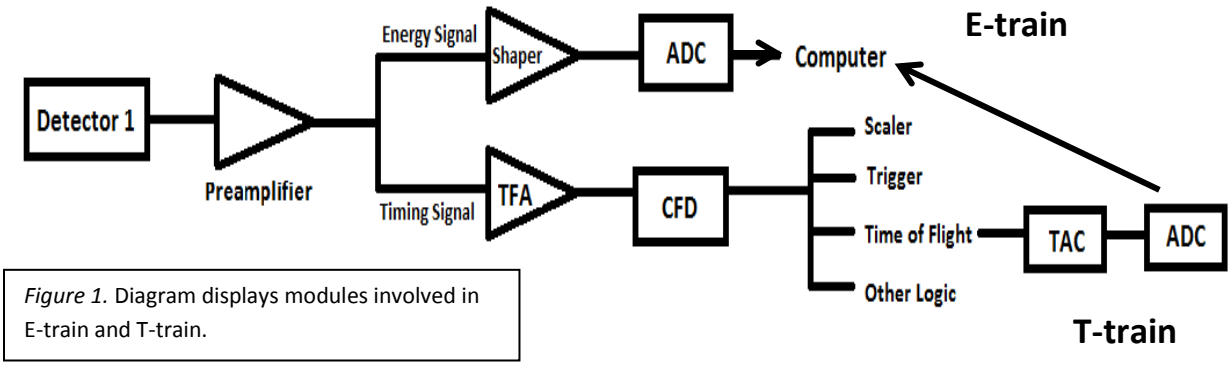


Figure 1. Diagram displays modules involved in E-train and T-train.

The energy signal is first slowly shaped into a peak with attributes that can easily be interpreted to have physical implications (i.e. amplitude, FWHM, area, centroid). The amplitude of the peak is digitized by the Analog-to-Digital-Converter (ADC) for computer display. The timing signal, on the other hand, is first amplified by the Timing Filter

Amplifier (TFA) until the threshold is reached. This will trigger a square wave signal in the CFD module. The time-of-flight information inherent in the signal is then relayed to two separate converters, the TAC and the ADC, which together effectively act as a time-to-digital converter[1]. This signal is now digitized for computer display.

1.2 Germanium and Silicon Particle Detectors

In the traditional setup for particle detection systems, every channel on a silicon- or germanium-based particle detector requires each of the modules previously discussed in order to process the information sent from the detector. The traditional setup works well for experiments that require extremely high energy resolution of the generated peaks. This is because the noise level is inherently low in this setup, so the SNR can be kept above 1.0 when used with either a silicon- or germanium-based detector. High-purity germanium detectors are able to produce better energy resolution (displayed as FWHM) than silicon detectors, but also generally produce more unwanted noise. Consequently, the noise of the signal-processing setup must be at an inherently low level in order for the SNR of a high-resolution germanium detector to be kept above 1.0. High-purity germanium detectors are commonly used for experiments involving gamma-ray spectroscopy, as the natural range for y-rays emitted by nuclei is 0.1-20 MeV, and high resolution is necessary.

Silicon-based particle detectors are able to determine the position of particles within 10 µm and have a time response of 25 ns. Silicon detectors can be made to be highly segmented into several narrow strips, and arranged in an array of the desired geometry. Each strip on the detector corresponds to several channels; the channel processes the electric signals delivered by the conducting strip after a particle collides with the detector. A silicon detector's capacity for high segmentation allows for very accurate measurements of a particle's position.



Figure 2. Silicon Detector (YY1) Manufactured by Micron Semiconductor, Ltd. Notice there are 16 distinct single-sided silicon strip detectors arranged radially. Six of these units can be placed in a "lampshade" arrangement to cover a large angular range.

Each individual silicon detector (e.g., YY1 shown in Figure 2) may possess a relatively large surface area, and multiple detectors can be used in an array to span a large angular range within a chamber. This setup is useful for tracking a particle's trajectory after a collision event[4]. The use of multiple detectors, however, means there are often several hundreds of channels producing signals. These signals must somehow be amplified, shaped, and converted to a digital format before they can be interpreted.

1.3 The ASIC System and its Benefits

The University of Notre Dame has been working in collaboration with Indiana University to develop a silicon detector array of its own, known as SAND (Silicon Array at Notre Dame). SAND will be used for experiments examining phenomena such as carbon

burning, the ap process, and CNO breakout. SAND requires a readout of 240 channels that the ND ASIC system will provide[2].

Typically, the cost per channel of a commercial ADC is in the range of $150[1]. When running experiments that require data from several hundreds of channels, ADCs and TDCs become very expensive. So expensive, in fact, those experiments – when run in the traditional electronic readout setup – are not viable options for laboratories on a modest budget. An experiment run with SAND, for example, would cost the university upwards of $200,000.

The Application Specific Integrated Circuit (ASIC) setup for silicon detector arrays was developed in 2005 and is a much cheaper alternative to the conventional readout setup. The ASIC system is also far more compact and requires fewer cables and modules. This system is currently being used by schools like MSU, IU, LSU, and TAMU.

#Channels	ASIC	Conventional (other cost not included)
512	$18.77k + <10k	$444.8k
256	$15.17k + <10k	$222.4k
160	$13.82k + <10k	$139k

Figure 3. Chart compares costs of the conventional readout setup to the Integrated Circuit setup.

The chip that will be used in the ASIC system for SAND is HINP16C. Each of the 16 channels of HINP16C consists of a charge-sensitive amplifier (CSA). The CSA output is split to feed energy and timing branches, both of which produce sparsified pulses that undergo off-chip digitation through a pipeline ADC[1]. A central common channel on HINP16C provides the bias for the 16 processing channels, contains the readout electronics, and contains the circuits used for configuring the 16 channels. In this way, signals from multiple channels can be processed by a single ADC unit.

The ASIC system at the University of Notre Dame implements a motherboard that has the capacity for 16 chipboards. There are 2 HINP16C chips per chipboard, and each chip contains 16 processing channels. In total, the ASIC system at Notre Dame allows researchers to use up to 512 channels to process the energy and timing signals produced by the detector, all within a box of approximately 40 x 15 x 10 cm in volume. A drawback to the ASIC setup is that the inherent noise level of the entire system is increased. This doesn't present a significant problem for silicon detector arrays, but it does mean that the ASIC setup can't currently be used with high-resolution germanium detectors because the SNR could not feasibly be kept above 1.0 for an extended period of time.

2 Testing

2.1 Testing Linearity of HINP16C Preamplifiers

This summer we ran a variety of tests to determine certain attributes of the ASIC system. We examined the linearity of the HINP16C Preamplifiers by using the GUI and SpecTCL software while varying pulse [v] within the range of 0.025v to 3.6v. Centroids of the resulting peaks were measured using Xamine software. We recorded runs for all channels; 32 channels

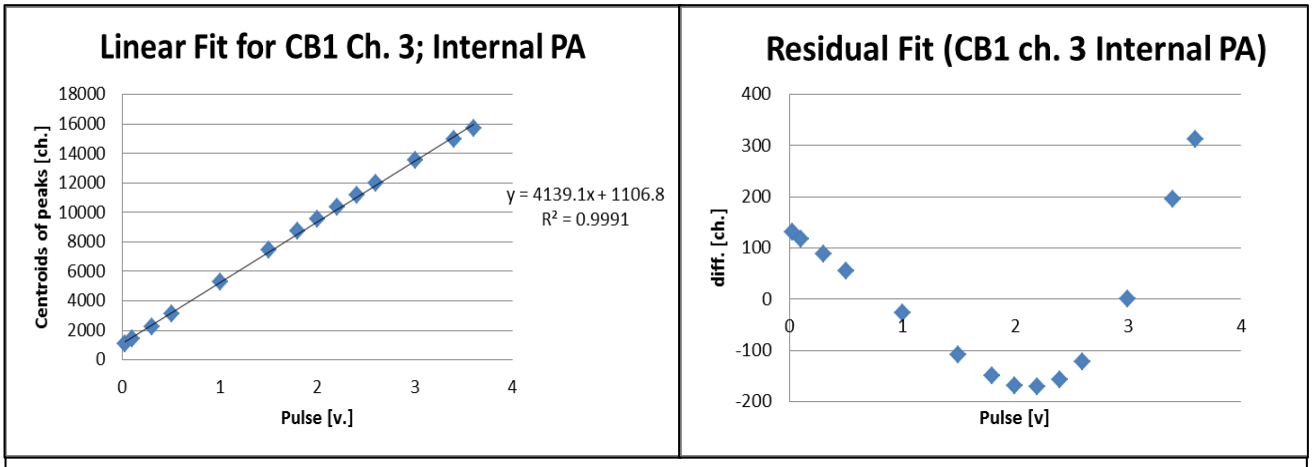


Figure 4. Linear and residual fits of runs recorded with Internal Preamplifier (IPA), Chipboard 1 (CB1), Channel 3. Results typical of all runs performed with IPA. Notice that residual fit is not randomized, but instead data follows a distinct curve.

per chipboard, chipboards 1-8. When the internal pre-amplifier of HINP16C was used, the runs produced data that showed poor linearity. This is shown by the residual fit of the data in Figure 4, which followed a distinct curve instead of being randomized.

The runs performed with the external preamplifiers, however, showed much stronger linearity. The pulse [v] was varied within the range of 0.04v to 3.3v, and the centroids [ch.] of the generated peaks were measured. As shown in Figure 5, the randomized residual fit and R^2 value of 1.00000 for this run indicate very strong linearity for the EPAs. A particle detection system with strong linearity can be calibrated using only 2 test points from an alpha source, whereas a system that is more accurately described by a polynomial fit, for example, requires far more test points to calibrate.

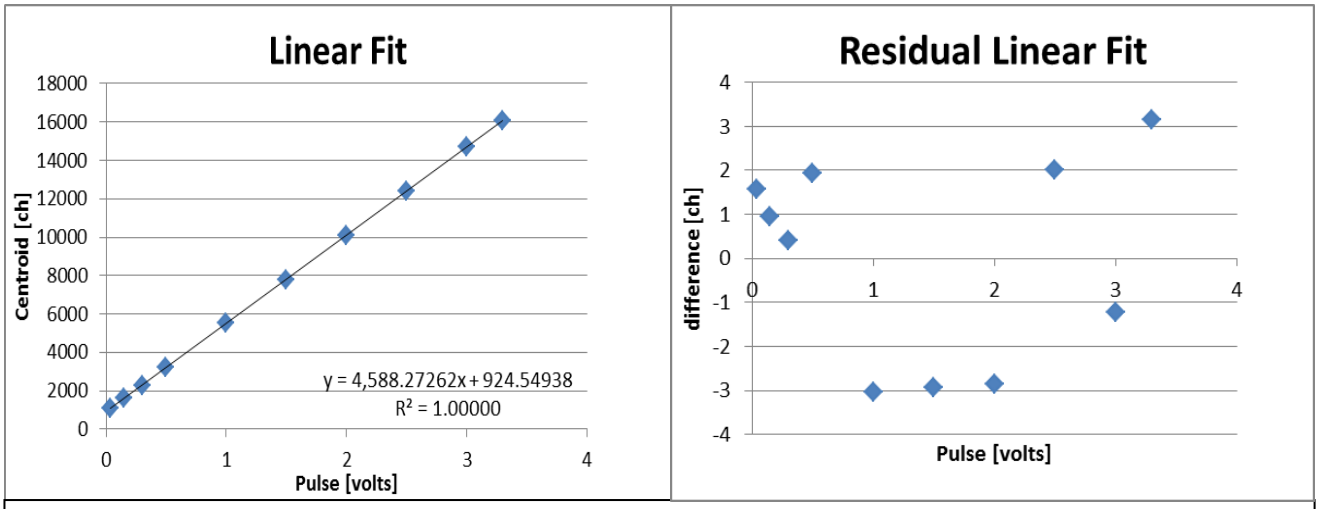


Figure 5. Linear and residual fits of runs recorded with External PA4, CB3, Channel 4. Results typical of runs performed with all External Preamplifiers (1-4). Data in residual fit appears to be randomized, indicating strong linearity of EPAs.

2.2 Energy Resolution of HINP16C

We recorded runs for 16 channels on CB3 for all external PAs, using ^{148}Gd and ^{241}Am as alpha sources. The resulting peaks were analyzed and the Centroid, FWHM, and Area were

recorded. Figure 6 shows a typical run for this setup. The peaks shown in Figure 6 possessed

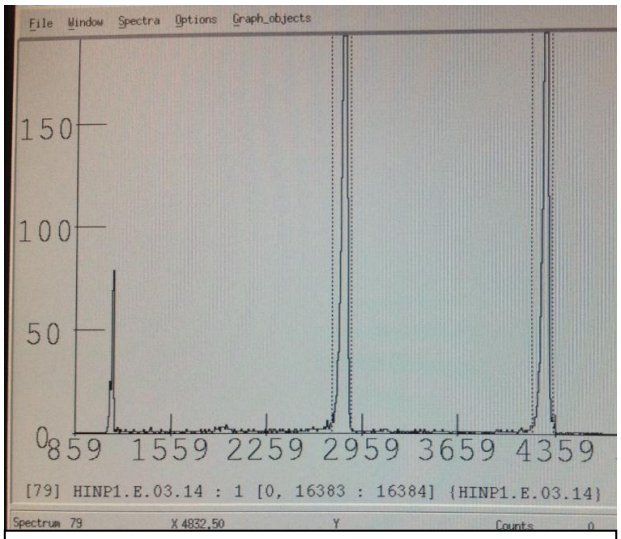


Figure 6. EPA4, CB3, Ch.14. Xamine display of run using ^{148}Gd and ^{241}Am alpha sources.

FWHMs of 49.277 channels and 47.685 channels (left to right). The standard definition for energy resolution is:

R = FWHM/Position of Peak

The energy resolutions of the peaks are 1.747% and 1.111%, respectively. The FWHM can be converted to energy (keV) by using the linear calibration of the channel. The resolutions of the peaks derived from the external preamplifiers were determined to be less than 30 keV[8].

2.3 Threshold Levels at Varying Discriminants

HINP16C threshold voltages were measured for chipboards 1-8 on channel 0. Channel 0 produced results typical of all channels. Discriminants were varied and results for each discriminant were recorded. Minimum threshold levels for HINP16C varied linearly with the discriminant setting on the Motherboard. Discriminants were adjusted in increments until noise levels became greater than the minimum threshold voltage. At this point the SpecTcl readout software

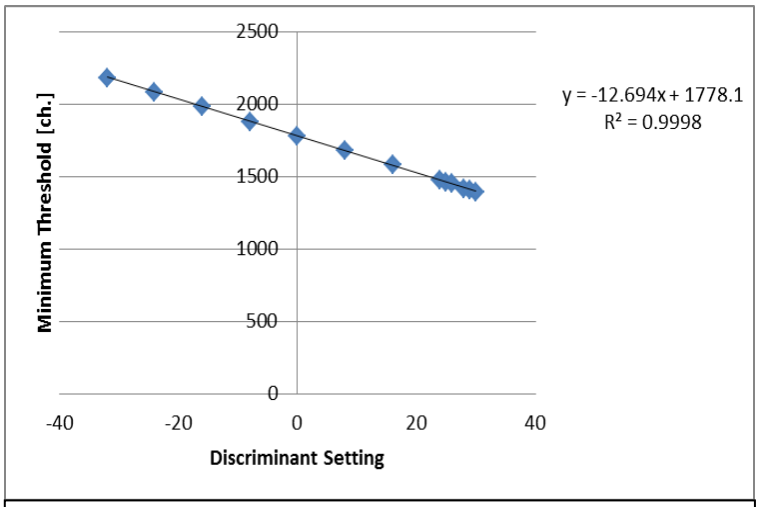


Figure 7. Minimum threshold levels at varying discriminants. Showed high linearity. Results typical of all chipboards.

would overload due to noise. The threshold at which this occurs allows one to determine noise levels inherent in the system for every chipboard that was tested.

3 Conclusion

Linearity, resolution, and quality of HINP16C in the ASIC system were tested. We have concluded that the internal preamplifier in HINP16C did not show strong linear character. The external preamplifiers, however, demonstrated strong linearity, with a typical R^2 value of 0.99999 for a linear fit. The external PAs will therefore be used with the ASIC system in future experiments.

Inherent noise levels varied by chipboard, but were found to be as low as 0.1986v (CB6, Ch.0, Discriminant set at -22). These results helped us to choose which type of cable would be connected to the silicon detector inside the particle chamber. There were two options: the stiff and expensive, but well shielded, coaxial cables, or the cheaper and more flexible option. We determined that the noise levels of the cheap and flexible cables were comparable to the coaxial cables, so they will be the ones used in future experiments.

4 References

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