Electronic Properties of Lead Telluride Quantum Wells

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Abstract

My research this summer has focused on measuring the electronic properties of quantum wells that combine two families of semiconductors, specifically Cadmium Telluride and Lead Telluride (CdTe/PbTe/CdTe), whose interfaces hold promise of Topological Crystalline Insulator (TCI) surface states. The samples used in my study are grown by Molecular Beam Epitaxy, and measured using Magneto Transport experiments. I have found that samples grown on higher temperature substrates have higher charge carrier mobilities and lower carrier concentrations, while the resistivity shows no significant change. These results will be used as a guide toward designing future structures for observing and characterizing TCI surface states.

Introduction

Semiconductors have many applications in electronic devices, and as these devices become smaller and smaller, so do their components. Hence the importance of understanding the complex surface states of semiconductors. Some of these surfaces are also possible examples of Topological Insulators (TIs) or Topological Crystalline Insulators (TCIs). By studying semiconductors in the form of thin films, quantum wells, nanowires, and quantum dots, researchers hope to better understand semiconductors in this form, to measure the electronic and magnetic properties of their surface states, and to discover new examples of TIs and TCIs. This summer I studied the electronic properties of Cadmium Telluride - Lead Telluride (CdTe/PbTe:Bi/CdTe) quantum well structures. The samples are grown by Molecular Beam Epitaxy, and measured using Magneto Transport. This paper focuses on the effects of differences in substrate temperature during growth on the resistivity, mobility, and carrier concentration of the quantum wells. Higher substrate temperature results in higher mobility, lower carrier concentration, and no significant change in resistivity.

Theoretical Background

Properties of Lead Telluride (PbTe)

Lead Telluride (PbTe) is a compound of the elements lead and tellurium. It forms in a rock-salt face-centered cubic crystal structure with ionic bonds. PbTe is a IV-VI narrow-gap semiconductor in the bulk.[7] This research compares the electrical properties of PbTe quantum wells (doped with Bi and sandwiched between CdTe layers) obtained with different growth conditions, and specifically using different substrate temperatures.

Topological Insulators and Topological Crystalline Insulators

Topological Insulators were predicted in 2005 and first confirmed experimentally in 2007.[6] The name refers to insulators which have a conducting surface state. TI band structure will show an energy gap between the valence and conduction bands, but will also have a thin surface or pathway connecting the two at certain points (this is the conducting surface state). On a 3-dimensional model of the band structure, the conducting surface looks like two cones in momentum space joined at their apices. The cones are called Dirac cones, and the point where they meet is the Dirac point. This contact/crossing of the valence and conduction bands is a consequence of the interface between a semiconductor and vacuum, or between two semiconductors. The theory is complex, but most basically, the different topologies on either side of the interface require some sort of crossing or contact to switch between them. For a TCI, the crystal structure of certain faces contributes to this state, and it exists on some faces but not others.[2, 4-6]

Electrons flow along the conducting surfaces via the Quantum Spin Hall Effect (QSHE). The charges split up according to their spin, and move only in the direction perpendicular to that spin. They thus form four "traffic lanes," one for each direction on two edges of the surface. When the electrons are flowing in their "lanes," their motion is locked to their spin. Therefore, even if they hit an impurity, they cannot change direction, and so they go around it. This greatly reduces scattering in the material, which means conduction on TIs and TCIs is significantly more efficient.[2, 4-6]

Because of the inherent dependence of these effects on spin, TIs and TCIs have potential applications in spintronics, and especially for quantum computing.[5]

Fabrication of PbTe

Molecular Beam Epitaxy

We fabricate our samples using a Molecular Beam Epitaxy (MBE) machine. The MBE allows us to grow very specific compounds with certain ratios of elements, one atomic layer at a time. The sample grows on a substrate, which is inside an ultra-high vacuum chamber. The vacuum keeps the space inside the chamber free of stray atoms which could contaminate the growth. Heaters in the MBE machine heat elemental sources until the elements are in gaseous form. The elements are then released into the chamber by opening and closing shutters in appropriate amounts, as needed. The beams of particles are all aimed at the substrate target. A Reflection High-Energy Electron Diffraction (RHEED) gun allows an observer to monitor the growth of the sample by checking the flatness of the surface being grown.

For the present growth of the (CdTe/PbTe:Bi/CdTe) quantum well structures, the growth times and temperatures of all the elements were the same for each sample, with only the substrate temperature varying. If the substrate temperature is too low, the crystal will form an imperfect structure, with surface imperfections which change the electronic structure and impede conduction. If the substrate temperature is too high, the layers will diffuse into each other, blurring the boundaries which keep the electrons inside the quantum well. Theoretically, the samples yield the best data (with better conduction and lower background noise) at some temperature between these two extremes.

Growing PbTe on CdTe

As shown in figure 1, the samples consist of a Lead Telluride (PbTe) quantum well doped with Bi, between two thicker layers of Cadmium Telluride (CdTe), all on a substrate of Gallium Arsenide (GaAs). PbTe and CdTe have similar lattice constants (less than 1% mismatch) and similar structures (they are both face centered cubic), so they can form covalent bonds at the interface. The PbTe and CdTe crystals both have polar and nonpolar faces. Of the five ways they can bond, one bonds between

the two non-polar surfaces, two between a polar and a nonpolar surface, and two bond between two polar surfaces.[3, 7]

Crystallographic Structure Diagram

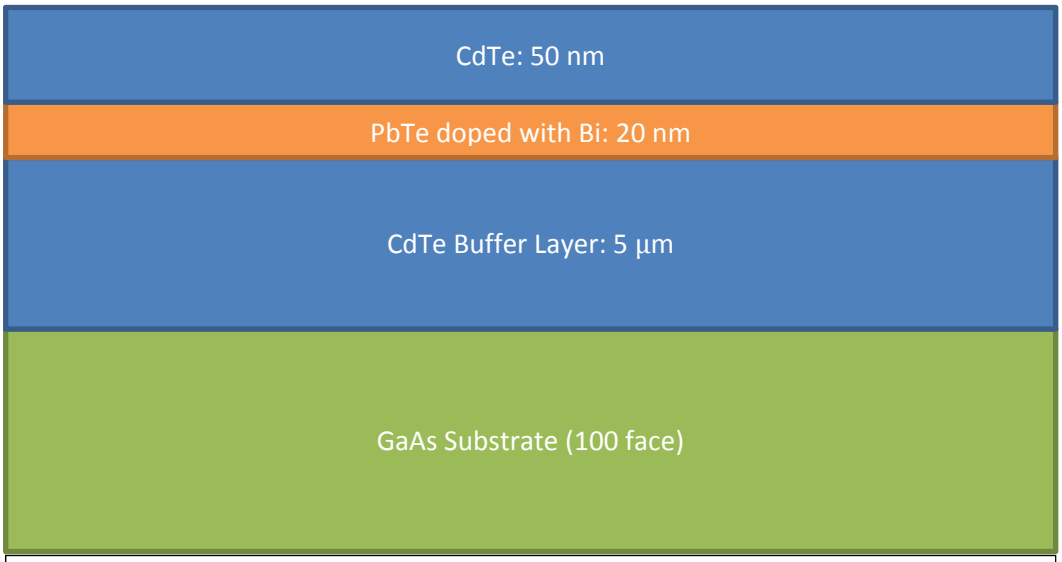

Figure 1: Diagram of sample structure. All samples were grown on a Gallium Arsenide wafer (100 face), followed by a Cadmium Telluride buffer layer 5 microns thick, then the Lead Telluride quantum well doped with Bismuth (20 nm), and finally a 50 nm layer of Cadmium Telluride.

Magneto-Transport

Method

Magneto-Transport measures the sheet resistance and hall resistance of the sample at varying magnetic field strengths and different temperatures from 300K to 16K. From the sheet resistance we can calculate the resistivity of the samples at different temperatures. From the hall resistance data, we can calculate carrier concentration and mobility, using the following equations. Charge Carrier Concentration $n = \frac{BI}{V_h de}$, where $\frac{BI}{V_h}$ is the inverse slope of the Hall Resistance versus Field plot, d is the thickness of the quantum well, and e is the charge of an election. Resistivity $\rho = RS/l$, where R is the sheet resistance, S is the product of the sample width and thickness d, and l is the sample length. Charge Carrier Mobility $\mu = 1/\rho ne$. Charge Carrier Type is determined by the sign of the slope of the

Hall Resistance versus Field plot: a negative slope indicates electrons, and a positive slope indicates holes.

Results

Carrier Concentration

Figure 2 shows the plot of carrier concentration versus substrate temperature during growth. We found a negative relationship between the substrate temperature during sample growth and the carrier concentration of the sample. Samples grown on a higher temperature substrate had lower carrier concentrations when measured at 30K (in blue), 20K (in green), and 16K (in orange). These data for all three temperatures agree very well, and show the same relationship.

The carrier type data was the same for nearly all the samples. The samples grown at the lowest temperature, 250C, sometimes produce positive charge carriers, and at other times negative charge carriers. All samples at higher temperatures, however, consistently had negative charge carriers.

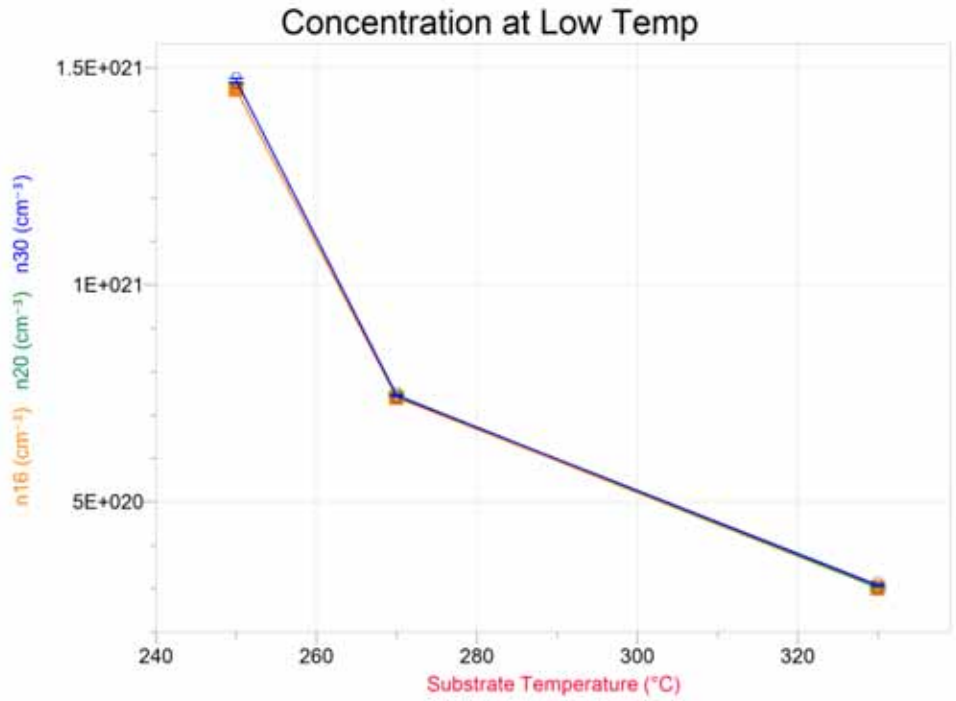

Figure 2: Plot of Carrier Concentration versus Substrate Temperature. Data taken at 30K (in blue), 20K (in green) and 16K (in orange).

Resistivity

Figure 3 shows the plot of sample resistivity versus substrate temperature. The data showed no significant difference in resistivity between samples grown at different substrate temperatures. The resistivities of the samples grown at different temperatures are all comparable to each other; the differences between the values are well within the error limits for each measurement.

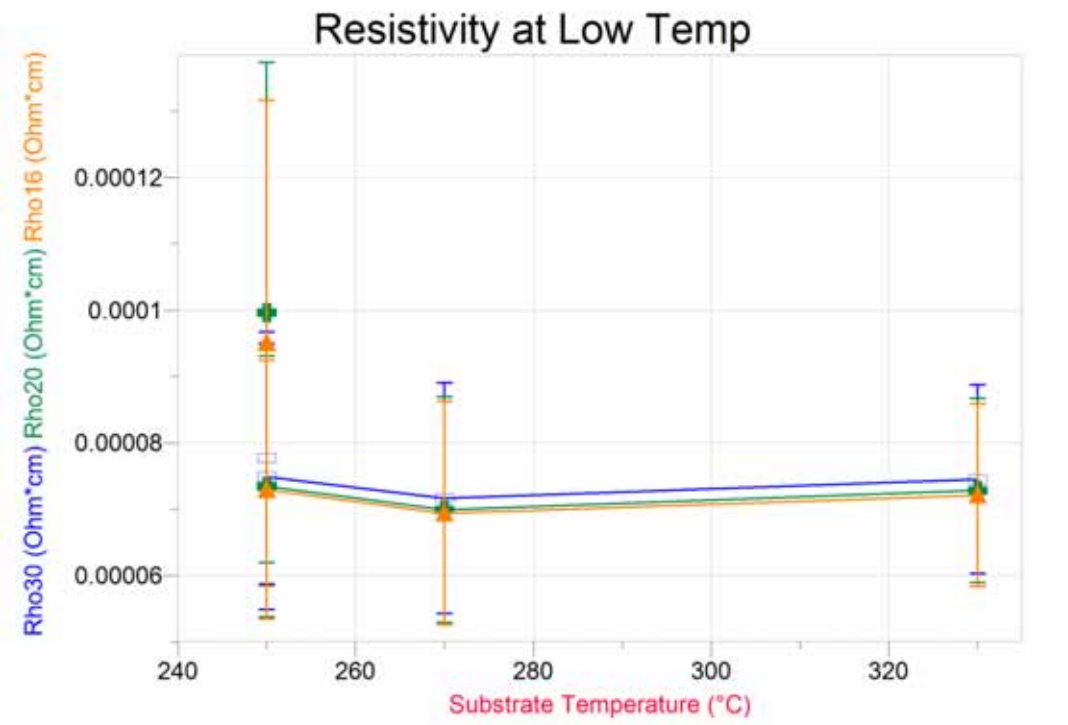

Figure 3: Plot of Resistivity versus Substrate Temperature. Data taken at 30K (in blue), 20K (in green) and 16K (in orange).

Charge Carrier Mobility

Figure 4 shows the plot of carrier mobility versus substrate temperature. We found a positive relationship between substrate temperature during sample growth and charge carrier mobility in the sample. The samples grown at higher substrate temperatures had higher charge carrier mobilities when measured at low temperature. The data taken at different temperatures agree well with each other, all showing the same trend.

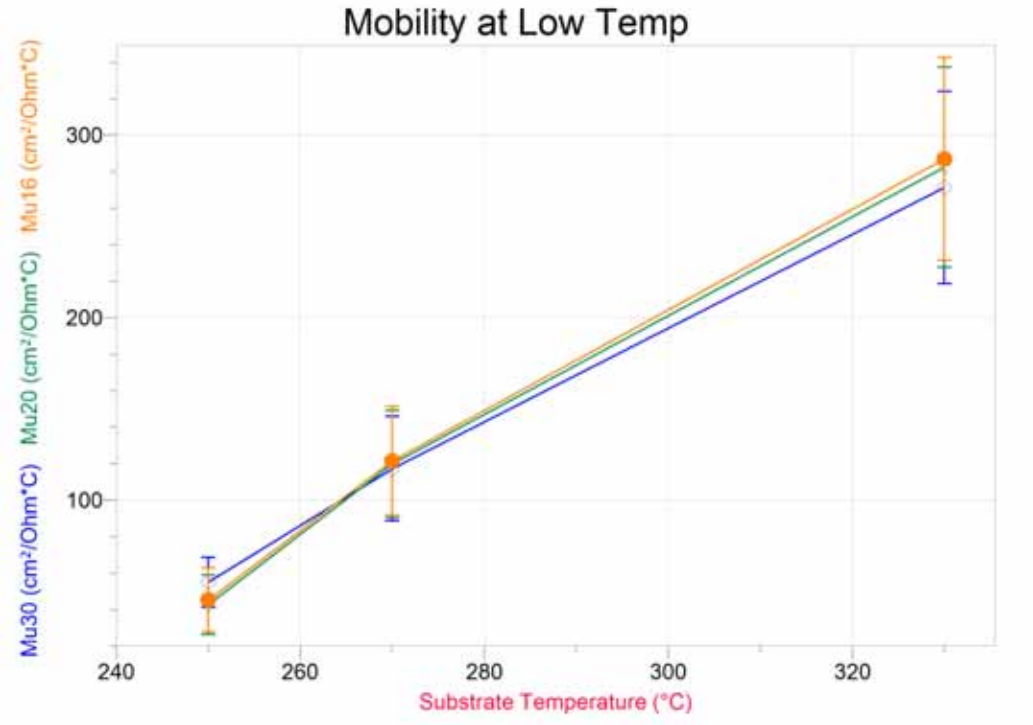

Figure 4: Plot of Carrier Mobility versus Substrate Temperature. Data taken at 30K (in blue), 20K (in green) and 16K (in orange).

Since the resistivity of all samples showed no significant differences, we suspect that the different substrate temperatures did not cause significant structural changes in the material which would impede conduction. Rather, it is likely that the higher carrier concentrations in the lower temperature samples led to the lower carrier mobility in those same samples. Carrier mobility is a measure of the mean free path of a carrier, namely, how far the carrier can travel before hitting an impurity or another carrier. When the density of charge carriers is higher, the mean free path is decreased because they bump into each other more often. In the same way, the higher temperature sample had a higher mobility because of its lower carrier concentration.

Conclusions

This research focused on determining the effects of differences in substrate temperature during growth on the properties of lead telluride quantum wells. The samples grown by molecular beam epitaxy consisted of lead telluride doped with bismuth, between two layers of cadmium telluride, all on

a substrate of gallium arsenide. From the Magneto-Transport study, we concluded that higher substrate temperatures result in lower charge carrier concentration, higher charge carrier mobility, and no significant difference in resistivity. The inverse relationship between carrier concentration (determined by substrate temperature) and carrier mobility indicates that lowering the carrier concentration increases the mean free path of the charge carriers, and thus their mobility.

This research revealed an important connection between substrate temperature, carrier concentration, and carrier mobility. Furthermore, the fact that the product of these values remains the same in all measurements, i.e., higher carrier concentrations lead to higher scattering rates, strongly suggests the scattering is dominated by carrier-carrier interaction; or, alternatively, that it is dominated by the scattering of the carriers on impurities responsible for generating carriers in PbTe. Since for every carrier there is a dopant or defect that produces it, the more carriers you have, the more ionized dopants they leave behind, and carriers can scatter on those. From this we can conclude that increasing the number of carriers alone is not sufficient for achieving lower resistivities.

This conclusion is an important insight into the properties of PbTe-base quantum structures, and provides more information about the optimal growth conditions for these structures. Continuing to fabricate better lead telluride quantum wells, and then using those quantum wells to look for topological insulator characteristics, is the next step for the research.

References

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